Marked up version of the Specification, showing changes made:

Page 8, lines 17-18:

More specifically, the areas covered by the layer of nitride [110] 120 will not react and will not oxidize during the steps of the STI process and the LOCOS process.

Marked up version of the claims:

Please add claims 18-22, as follows:

18. (New) A semiconductor device, comprising:
a common substrate;
a first region formed on the common substrate, the first region comprising an SRAM device, a first active region, and a first isolation region having a first isolation structure, the SRAM device overlying the first active region, the first active region isolated by the first isolation region, the first active region and the first isolation region forming a uniform region made of a first material; and
a second region formed on the common substrate, the second region comprising a flash EPROM device, a second active region, and a second isolation region having a second isolation structure, the flash EPROM device overlying the second active region, the second active region isolated by the second isolation region, the second active region and the second isolation region forming a uniform region made of a second material,
wherein the first isolation structure is different from the second isolation structure.

19. (New) The semiconductor device of claim 18, wherein the first isolation structure is a shallow trench.

20. (New) The semiconductor device of claim 18, wherein the second isolation structure is a LOCOS isolation structure.

21. (New) The semiconductor device of claim 18, wherein the first material comprises an insulating oxide.

22. (New) The semiconductor device of claim 18, wherein the second material comprises an insulating oxide.

REMARKS

The Applicant respectfully requests further examination and reconsideration in view of the amendments made above and the comments set forth fully below. Within the Office Action, the Claims 1-10 were rejected. By the above amendment, claims 18-22 have been added. Accordingly, claims 1-10 and 18-22 are pending.

Rejection under 35 U.S.C. § 112, first paragraph

Within the Office Action, claims 1-10 have been rejected under 35 U.S.C. 112, first paragraph. It is stated within the Office Action, "In this case the limitation 'wherein the first isolation technique and the second isolation technique are different and **implemented sequentially**' renders new matter situation" (emphasis and underlining in original). The Applicant respectfully disagrees with this assertion.

The claimed limitation "implemented sequentially" is not new matter; support for it can be found throughout the Specification as originally filed. For example, at page 4, lines 2-7 of the Specification, it is stated: "Preferably, the LOCOS isolation technique is first implemented to define a flash area of the silicon substrate on which the flash EPROM cell is implemented. . . . After the LOCOS isolation technique has been fully implemented, the flash area is then preferably masked and the STI technique is implemented in order to define the SRAM area of the silicon substrate on which the SRAM cell is implemented"; at page 8, lines 21-22: "In the preferred embodiment, the LOCOS isolation process is implemented on the substrate 100 before the STI process"; at page 9, lines 7-9: "Preferably after the LOCOS isolation process is completed, the STI process commences by forming a mask 170 over the second area 104 and an active region within the first area 102, as illustrated in Figure 10"; on page 10, lines 5-7: "In the preferred embodiment of the present invention, the LOCOS isolation process is implemented on the silicon substrate before the STI process"; and on page 10, lines 9-10: "In a first alternate embodiment, the STI process is implemented on the silicon substrate prior to the LOCOS isolation process."

Because the limitation "wherein the first isolation technique and the second isolation technique are different and implemented sequentially" (underlining added) is supported in the Specification as originally filed, the rejection under 35 U.S.C. § 112, first paragraph, is improper and should be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,605,853 to Yoo et al. (hereinafter "Yoo") in view of U.S. Patent No. 5,679,599 to Mehta (hereinafter "Mehta"). The Applicant respectfully disagrees with this rejection.

Yoo teaches a method of forming a SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously a SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. (Yoo, col 3, lines 51-55). Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. (Yoo, col 3, line 55-60). Yoo does not teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Neither does Yoo teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a combination of a LOCOS and an STI isolation process.

Mehta teaches a device and method for isolating regions of the circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. (Mehta, Abstract and col. 4, line 46- col. 6, line 49). Mehta teaches a method of combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which ***simultaneously*** forms a portion of the LOCOS region and trench isolation structure. (Mehta, col 4, line 47-51). However, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *sequentially* forms a portion of the LOCOS region and trench isolation structure. Furthermore, Mehta does not teach a separation technique for growing flash EPROM and SRAM on a common substrate.

The present invention is directed to a system for and method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate including an area on the silicon substrate where a local oxidation of silicon (LOCOS) isolation technique is implemented and another area on the same silicon substrate where a shallow trench isolation (STI) technique is implemented. (Specification, Abstract). The present invention teaches a system for *independently* or *sequentially* integrating SRAM cells and flash EPROM cells onto a single silicon substrate.

As discussed above, Yoo does not teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process. Within the Office Action, it is acknowledged that Yoo et al. do not expressly disclose a second isolation technique such as STI to isolate the devices.

Also, as discussed above, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *sequentially* forms a portion of the LOCOS region and trench isolation region. Nor does Mehta teach a separation technique for growing flash EPROM and SRAM on a common substrate. Accordingly, neither Yoo, Mehta nor their combination teach or suggest a system for independently or sequentially integrating SRAM cells and flash EPROM cells onto a single silicon substrate. Further, neither Yoo, Mehta nor their combination teach or suggest forming a SRAM and an EEPROM on a single substrate using a combination of a LOCOS and an STI isolation process.

Within the Office Action, it is stated that "Mehta, in fig. 8, teaches a first and second isolation techniques 242, 240 to separate the devices in the same substrate in order to scale the minimum spacing between regions" (citing Mehta, col. 6, last paragraph). It is then concluded that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use STI isolation technique as taught by Mehta in Yoo et al. substrate in order to scale the minimum spacing between regions." The Applicant respectfully disagrees with this conclusion.

To support this conclusion, the Office Action must demonstrate a *prima facie* case of obviousness. No demonstration has been made here. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of the references. Second, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Third, the combination of the prior art references must teach or suggest all the claim limitations. [M.P.E.P § 2142 - 43.]

First, within the Office Action, there is no suggestion or motivation to combine Yoo and Mehta. As discussed more fully below, Yoo teaches away from including a SRAM and an EPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second

isolation techniques can be applied to isolate a SRAM and an EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1420 (Fed. Cir. 1990). Within the Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo or Mehta suggesting the desirability of combining these two references.

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of a SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation techniques can be applied to isolate a SRAM and an EPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *sequentially* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, Yoo nor their combination teaches or suggests forming a SRAM and an EPROM on a single substrate using a combination of a LOCOS and STI isolation process. In column 2, lines 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining a SRAM and an EEPROM on the same IC, when the <u>same</u> LOCOS isolation process is used on <u>all</u> the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating a SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skilled in the art, that Yoo could have been

combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate. Therefore it would not have been obvious to one skilled in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form a SRAM and an EEPROM on a common substrate.

The independent Claim 1 is directed to a semiconductor device. The semiconductor device of Claim 1 comprises a common substrate, an SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM device implemented on the common substrate and isolated by a second isolation technique. It is specified in Claim 1 that the first isolation technique and the second isolation technique are different and implemented sequentially. As described above, neither Mehta, Yoo nor their combination, teach or suggest an SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. Further, neither Mehta, Yoo nor their combination teach that the first isolation technique and the second isolation technique are different and implemented sequentially. For at least these reasons, the independent Claim 1 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 2, 3 and 4 are dependent on the independent claim 1. As discussed above, the independent claim 1 is allowable over the teachings of Yoo, Mehta, and their combination. Claims 2, 3 and 4 are therefore allowable as being dependent on an allowable base claim.

The independent Claim 5 is directed to a system for allowing different types of isolation techniques during fabrication of a semiconductor device. The system of Claim 5 comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing. It is specified in Claim 5 that the first isolation technique and the second isolation technique are different and implemented sequentially. The system of Claim 5 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device, implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. As further discussed above, neither Mehta, Yoo nor their combination teach that the first isolation technique and the second isolation technique are different and implemented

sequentially. For at least these reasons, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 6, 7, and 8 are all dependent on the independent Claim 5. As discussed above, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claims 6, 7 and 8 are also allowable as being dependent on an allowable base claim.

The independent Claim 9 is directed to a semiconductor device comprising a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing. It is specified in Claim 9 that the STI isolation technique and the LOCOS isolation technique are implemented sequentially. The device of Claim 9 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device implemented on the second portion of the substrate. As described above, neither Mehta, Yoo, nor their combination teach implementing an SRAM device, isolated by an STI technique, on a common substrate with a flash EPROM device, isolated by a LOCOS isolation technique. As further discussed above, neither Mehta, Yoo nor their combination teach that the STI isolation technique and the LOCOS isolation technique are implemented sequentially. For at least these reasons, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination.

Claim 10 is dependent on the independent Claim 9. As discussed above, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claim 10 is also allowable as being dependent on an allowable base claim.

Within the Office Action, *In re Thorpe*, 777 F.2d 695, 227 U.S.P.Q. 964 (Fed. Cir. 1985), is cited for the assertion that the process limitation "implemented sequentially" recited in claims 1, 5, and 9 "would not carry any patentable weight in this claim drawn to structure." Reliance on *Thorpe* is misplaced. In *Thorpe*, claim 1 was a process claim. 777. F.2d at 696. Claim 44, which was rejected, recited no structural limitations, claiming "The product of the process of Claim 1." *Id.* In contrast, claims of the present invention recite structure that is *further defined* by process limitations. For example, claim 1 of the present invention claims a common substrate; an SRAM device implemented on the common substrate and isolated by a first isolation technique; and a flash EPROM device implemented on the common substrate and isolated by a second isolation technique. Furthermore, the first isolation technique and the second isolation technique are different and implemented sequentially.

Claim 1, unlike the claim rejected in *Thorpe*, recites structure further defined by process steps. Accordingly, *Thorpe* does not teach against the limitations recited in claim 1.

Similarly, claims 5 and 9 also recite structure further defined by process limitations. For these reasons, claims 1, 5, and 9 are allowable in light of *Thorpe*.

As illustrated above, the Applicant has described both Yoo and Mehta, discussed the application of each, and argued why neither, alone or in combination, taught or suggested the invention claimed in the present application. Nevertheless, within the Office Action, the scope of the Applicant's arguments is ignored. As stated within the Office Action:

> For instance, in response to the applicant's [read, Examiner's] arguments, on pages 5-6, the applicant repeatedly submits, "Yoo does not teach or suggest that SRAM and an EEPROM can be formed on the same IC, using non-LOCOS isolation process, such as a shallow isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process." As addressed in the previous Office Action, [t]he combination of Yoo and Mehta teaches the technique of using LOCOS and STI isolations. The LOCOS and STI apparently are different. Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

This is a mischaracterization of the Applicant's arguments. Within the Office Action it is suggested that the Applicant argued only that Yoo does not disclose the claimed invention. As discussed above, however, the Applicant has argued and herein argues that neither Yoo nor Mehta, alone *or in combination*, teaches or suggests the claimed invention.

For this reason, the reliance on *Keller* and *Merck* within the Office Action is misplaced. In both *Keller* and *Merck*, the applicant tried to overcome a § 103 rejection by arguing that one reference did not teach a limitation taught in the pending application. In contrast, here the Applicant has described why the *combination* of references neither teaches nor suggests the claims in the present invention. Accordingly, the rejection of the independent claims 1, 5, and 9 is improper, and claims 1, 5, and 9 are allowable.

It is next stated within the Office Action:

> [The] applicant argues about claim limitations of a method of making the device, on pages 5-6. It is noted that applicant elected the device claims in the previous amendment, paper 15. The method claims, Group II, therefore has [sic] been withdrawn from examination. Therefore, the discussion regarding limitations in the method of making the device has nothing to do with the previous Official Action, nor this paper. The newly added limitation such as implemented sequentially also is [a] process limitation, see above discussions.

The Applicant respectfully disagrees with this conclusion for at least two reasons. First, the Applicant described the method of making the device to prove that neither Yoo nor Mehta, either alone or in combination, teaches how to make the present invention and thus cannot teach or suggest any combination that would produce the present invention. As stated in the Response to Office Action Mailed on May 6, 2002:

> The discussion within the previous Responses on the limitations of the LOCOS and STI isolation techniques is relevant since it limits the applicability of the teachings of Yoo in view of Mehta, to the present invention. It is relevant because, without incorporating two separate techniques independently or sequentially, neither Yoo, Mehta, nor their combination can teach the claimed invention, which expressly teaches the incorporation of two separate techniques in the fabrication of the claimed invention.

The Applicant disagrees with the conclusion for a second reason: The MPEP itself allows product-by-process claims: "A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper." MPEP § 2173.05(p)(I) (8th ed. 2001).

The new claims 18-22

The new claim 18 recites structure neither taught nor suggested by the cited prior art. Claim 18 recites a common substrate and a first region and second region, both formed on the common substrate. The first region comprises an SRAM device, a first active region, and a first isolation region having a first isolation structure. The SRAM device overlies the first active region, which is isolated by the first isolation region. The first active region and the first isolation region form a continuous region made of a first material. The second region comprises a flash EPROM device, a second active region, and a second isolation region having a second isolation structure. The flash EPROM device overlies the second active region, which is isolated by the second isolation region. The second active region and the second isolation region form a continuous region made of a second material. Furthermore, the first isolation structure is different from the second isolation structure.

Because claim 18 recites limitations not disclosed in any of the cited prior art references, it is allowable over the cited prior art references. Because claims 19-22 depend from claim 18, they too are allowable over the cited prior art.

New claim 18 contains no new matter. Claim 18 finds support in the Specification as filed, at least at page 9, lines 3-6 and 17-24. Moreover, claims 19-22 contain no new matter.

Claims 19 and 21 find support in the Specification as filed, at least at page 9, lines 12-20. Claims 20 and 22 find support in the Specification as filed, at least at page 9, lines 3-6.

For the reasons given above, the Applicant respectfully submits that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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